REMARKS

1. Amendments to the claims

Claims 1-3 and 5 have been amended to rename the term 'sustaining electrode' to *'auxiliary electrode'* as disclosed, for example, at page 4, line 30 of the application as filed. Additionally, claim 1 has been amended to recite that the pixel electrode has an edge and that the edge of the pixel electrode is disposed on the auxiliary electrode, as disclosed, for example, at page 5, lines 8-9.

Claim 4 has been amended to recite that the pixel electrode is coupled to the source electrode via a contact hole as disclosed, for example, at page 5, lines 3-5 of the application as filed.

Claim 6 has been amended to recite that the edge of the pixel electrode is disposed on the source electrode as disclosed, for example, at page 4, lines 16-17 of the application as filed.

New claims 10 and 11 have been introduced. Support for new claims 10 and 11 can be found in Figures 2A and 3A, and in the related portion of the specification.

Applicant submits that no new matter has been introduced.

2. Specification

In section 1 of the Action, the Examiner has requested page 1 lines 30-31 to be corrected to indicate that number 12 shows a source electrode, and not a drain electrode. Applicant has now complied with this requirement, as shown in the section "In The Specification" above.

3. Drawings

In section 2 of the Action the Examiner has objected to the drawings under 37 CFR 1.83(a), requiring the drawings to show every feature of the invention specified in the claims. In particular, the Examiner has requested that the feature that the pixel electrode is coupled to the pixel electrode via a contact hole must be shown or the feature canceled from the claims. Applicant has cancelled the feature from the claims by amending claim 4 and deleting claim 9. In claim 4 as amended, "*the pixel electrode is coupled to the source electrode via a contact hole.*" Coupling of the pixel electrode to the source electrode via a contact hole is shown both in Figure 2A and Figure 3. Therefore, Applicant submits that the objection has been overcome.

Additionally, Applicant has amended Figure 2A to show section lines II-II and III-III, and amended Figure 3 to rename it as Figure 3A and to show section lines IV-IV and V-V. Furthermore, Applicant has introduced new Figures 2C, 3B, and 3C, to better clarify the claimed structure. Figure 2C is similar to Figure 2B, the only difference being the presence of a second cross sectional view of element 20c and a second cross sectional view of element 28. The subject matter of Figures 3B and 3C is straightforward from the observation of Figure 3A. Applicant submits that no new matter has been added.

4. Claim rejections in view of Applicant's Admitted Prior Art

In section 3 of the Action, the Examiner has rejected claim 1 under 35 USC 103(a) as being unpatentable over Applicant's Admitted Prior Art (APA). Applicant has now amended claim 1 and respectfully disagrees with the conclusions of the Examiner.

Claim 1 recites an '*auxiliary electrode.*' The auxiliary electrode is disclosed, for example, in Figure 3, where is shown as element 30. Applicant's APA does not disclose an auxiliary electrode. Applicant's APA discloses a source electrode, see element 12 of Figure 1A,

which is equivalent to the source electrode 21 of Figure 3A. Additionally, claim 1 recites that the pixel electrode has an edge and that "*the edge of the pixel electrode is disposed on the auxiliary electrode*." Applicant's APA does not disclose an auxiliary electrode, so that there is no disclosure that the edge of the pixel electrode is disposed on an auxiliary electrode.

Applicant submits that it would not be obvious for a person skilled in the art to provide the claimed TFT structure with an auxiliary electrode so that the edge of the pixel electrode is disposed on the auxiliary electrode, because Applicant's APA neither discloses nor supports the presence of an auxiliary electrode. Additionally, Applicant points out that the presence of an auxiliary electrode so that the edge of the pixel electrode is disposed on the auxiliary electrode allows the capacitance-coupling effect generated between the pixel electrode (see, for example, element 26 in Figure 3A) and the data line (see, for example, element 22 in Figure 2A) to be the same as that generated between the auxiliary electrode and the data line, as disclosed, for example, at page 6, lines 5-8 of the present application. Therefore, Applicant submits that claim 1 is patentable over Applicant's APA. Should the Examiner believe that additional prior art can be combined with Applicant's APA, he is respectfully requested to point out this prior art to the Applicant in detail.

In sections 4-6 of the Action, the Examiner has rejected claims 2 , 4, and 5 as obvious over Applicant's APA. Applicant has already shown that claim 1 as amended is patentable over Applicant's APA. Therefore, claims 2, 4, and 5 are deemed to be patentable over Applicant's APA at least in view of their dependency on claim 1.

In section 7 of the Action, the Examiner has rejected claim 6 under 35 USC 103(a) as being unpatentable over Applicant's APA. Applicant has now amended claim 6 and respectfully disagrees with the conclusions of the Examiner. In particular, although

Applicant's APA discloses a source electrode, Applicant's APA does not disclose a source electrode *"which is extended to the region where the pixel electrode is next to the data line"* and *"wherein the edge of the pixel electrode is disposed on the source electrode."* In particular, in Applicant's APA the source electrode is not extended to the region where the pixel electrode is next to the data line. In Applicant's APA the source electrode (see, for example, electrode 12 of Fig. 1A) is distant from a region where the pixel electrode is next to the data line. By contrast, Applicant's extended source electrode is disclosed, for example, in Figure 2A, where is shown as element 20c. Figure 2A shows that the source electrode is extended to a region where the pixel electrode is next to the data line. The Examiner can ascertain this by simple comparison between Figure 1A and Figure 2A. Also in this case, the capacitance-coupling effect generated between the pixel electrode and the data line is the same as that generated between the auxiliary electrode and the data line. Applicant submits that claim 6 is patentable over Applicant's APA. Should the Examiner believe that additional prior art can be combined with Applicant's APA, he is respectfully requested to show this prior art to the Applicant in detail.

In section 8 of the Action, the Examiner has rejected claim 7 as obvious over Applicant's APA. Applicant has already shown above that claim 6 as amended is patentable over Applicant's APA. Therefore, claim 7 is deemed to be patentable over Applicant's APA at least in view of its dependency on claim 6.

With reference to the Examiner's rejection of claim 9 in section 9 of the Action, Applicant has now cancelled claim 9, thus rendering moot the rejection of the Examiner.

5. Claim rejections in view of U.S. Pat. No. 5,737,051 to Kondo et al.

In section 10 of the Action, the Examiner has rejected claim 1 under 35 USC 103(a) as being unpatentable over Kondo. Applicant respectfully disagrees, substantially for the same reasons as set forth above with respect to claim 1. Claim 1 recites an *'auxiliary*

electrode' such that "*the edge of the pixel electrode is disposed on the auxiliary electrode*. In section 10 of the Action, when looking at Kondo, the Examiner is apparently making reference to element 1 at column 14, lines 1-2 of Kondo. However, the element 1 in Kondo is the pixel electrode. Additionally, the paragraph bridging column 13 and 14 in Kondo does neither disclose an auxiliary electrode, nor that the edge of the pixel electrode 1 is disposed on an auxiliary electrode. Therefore, Applicant believes that claim 1 is patentable over Kondo. Should the Examiner believe that additional prior art can be combined with Kondo against claim 1, he is respectfully requested to show this prior art to the Applicant in detail.

In sections 11 and 12 of the Action, the Examiner has rejected claims 2 and 3 as obvious over Kondo. Claims 2 and 3 depend on claim 1. Applicant has already shown above that claim 1 as amended is patentable over Kondo. Therefore, claims 2 and 3 are deemed to be patentable over Kondo at least in view of their dependency on claim 1.

6. Claim rejections in view of a combination between Applicant's APA and Kondo

In sections 13 to 18 of the Action the Examiner has rejected claims 4-9 as being unpatentable over Kondo in view of Applicant's APA. Applicant respectfully disagrees. Claims 4 and 5 depend on claim 1, which recites an '*auxiliary electrode*' such that "*the edge of the pixel electrode is disposed on the auxiliary electrode*. Applicant has already pointed out, in sections 4 and 5 above, that neither Applicant's APA nor Kondo disclose an '*auxiliary electrode*' such that "*the edge of the pixel electrode is disposed on the auxiliary electrode.*

Additionally, the remaining claims 6-9 of the present application all disclose a source electrode "*wherein the edge of the pixel electrode is disposed on the source electrode which is extended to the region where the pixel electrode is next to the data line.*" Neither Applicant's APA nor Kondo disclose such feature, so that a combination of Applicant's APA and Kondo does not render the subject matter of claims 6-9 unpatentable.

Therefore, Applicant submits that claims 4-9 are patentable over a combination between Applicant's APA and Kondo. Should the Examiner assert the contrary, he is respectfully requested to show to the Applicant in detail where in the Applicant's APA or in Kondo the above italicized features are shown.

7. Added claims

New independent claims 10 and 11 have been added. The total number of claims of the present application is now ten and the total number of independent claims is four. Applicant encloses to the present response the required fee for the additional independent claim.

Claims 10 and 11 are believed to be patentable over the prior art cited by the Examiner for the following distinctive features: Claim 10 claims an auxiliary electrode such that the edge region of the pixel electrode is disposed on the auxiliary electrode. In claim 11, the source electrode comprises an extended portion extended to a region corresponding to the edge region of the pixel electrode, so that the edge region of the pixel electrode is disposed on the extended portion of the source electrode.

For the reasons explained above, favorable reconsideration of the present application is respectfully requested.

* * *

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

Respectfully submitted,

Ross A. Schmitt

Ross A. Schmitt
Reg. No. 42,529
LADAS & PARRY
5670 Wilshire Boulevard, suite 2100
Los Angeles, California 90036
(323) 934-2300

Enclosures - Annex A
Annex B
Postcard
Letter to Drawing Review Branch
Fee calculation sheet

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on November 13, 2002.

Ross A. Schmitt
(Name of Registered Representative)

Ross A. Schmitt

Signature

November 13, 2002
Date

ANNEX A

TITLE

THIN-FILM TRANSISTOR ARRAY STRUCTURE

BACKGROUND OF THE INVENTION

Field of the invention

This invention relates to a Thin-Film Transistor array structure. More particularly, this invention relates to a Thin-Film Transistor array structure for sustaining all capacitance-coupling effects between a source electrode and a data line of a panel.

Description of Prior Art

For the manufacture of a Thin-Film Transistor (TFT) array of a panel, especially in the case of those with a larger size, the exposure process on the TFT has to be divided and proceeded by several steps.

However, the alignment of the layers between each two adjacent exposed blocks of the TFT is easily dislocated during the exposure process, and the capacitance-coupling effects between a source electrode and a data line on each of the adjacent exposed blocks are very different. Thus, the penetrating rates of each block of the TFT are different in typical TFT structures.

Referring to Fig. 1A, Fig. 1A is a plan view showing the structure of one pixel of typical TFT structure. Symbol "CE" represents a common electrode, symbol "SL" represents a scanning line, symbol "10" represents a TFT, and symbol "DL" represents a data line. The ~~drain~~ source electrode 12 of the TFT 10 is coupled to an ITO electrode (i.e. pixel electrode) 16 via a contact hole 14 formed on an isolated layer, and the data line DL is coupled to a

drain electrode 18 of the TFT 10.

Fig. 1B is a cross-section according to a line I-I of Fig. 1A. A distance Δd existing between the data line DL and the ITO electrode 16 is formed during the exposure process and is an important parameter related to the capacitance-coupling effect of two adjacent blocks of the TFT 10. Once the distance Δd exceeds a predetermined value, the capacitance-coupling effect of the adjacent blocks is easily affected and causes a visible line on the panel.

SUMMARY OF THE INVENTION

To solve the above problem, the primary object of this invention is to provide a TFT array structure, which comprises a Thin-Film Transistor, a data line, a scanning line, a pixel electrode and an auxiliary electrode. The data line is connected to the drain of the Thin-Film Transistor, and the scanning line is connected to the gate of the Thin-Film Transistor. The scanning line is oriented substantially orthogonally with respect to the data line to form a plurality of rectangular pixels in matrix. The auxiliary electrode is formed at the place where the pixel electrode is close to the edge of the data line, and the auxiliary electrode is coupled to the pixel electrode and located at a mask on which the data line is located. The capacitance-coupling effect generated between the pixel electrode and the data line is the same as that generated between the predetermined electrode and the data line, and the performances of all pixels are uniform despite errors occurring during the aligning process on the pixel electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by

reading the subsequent detailed description and examples with reference made to the accompanying drawings in which:

Fig. 1A is a plan view showing the structure of one pixel of a typical TFT structure.

Fig. 1B is a cross-section according to a line I-I of Fig. 1A.

Fig. 2A is a plan view showing the structure of one pixel of a TFT structure according to one embodiment of the present invention.

Fig. 2B is a cross-section according to a line II-II of Fig. 2A. Fig. 2C is a cross-section according to a line III-III of Fig. 3A / Fig. 2A is a plan view showing the structure of one pixel of a TFT structure according to another embodiment of the present invention.

Fig. 3B is a cross section according to a line IV-IV of Fig. 3A.
Fig. 3C is a cross section according to a line V-V of Fig. 3A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 2A is a plan view showing the structure of one pixel of a TFT structure according to one embodiment of the present invention, and Fig. 2B is a cross-section according to a line II-II of Fig. 2A.

The TFT array structure comprises a Thin-Film Transistor 20, a data line 22, a scanning line 24, a pixel electrode 26 and a common electrode CE. The data line 22 is coupled to a drain electrode 20a of the Thin-Film Transistor 20, and the scanning line 24 is coupled to a gate electrode 20b of the Thin-Film Transistor 20 and crossed to the data line 22 to form a plurality of rectangular pixels in matrix. The pixel electrode 26 is constructed at each of the pixels and coupled to a source electrode of the Thin-Film Transistor 20 via a contact hole 28 which is formed on an isolated layer (not shown). A source electrode 20c of the Thin-Film Transistor 20 is extended to the region (both sides of the data line 22)

where the pixel electrode 26 is next to the data line 22, and the edge of the pixel electrode 26 is disposed onto the source electrode 20c.

Fig. 2B is a cross-section according to a sectional line II-II of Fig. 2A. In Fig. 2B, it is understood that the capacitance-coupling effect is mainly generated between the data line 22 and the source electrode 20c. As the source electrode 20c and the data line 22 are formed on the same mask and the pixel electrode 26 is coupled to the source electrode 20c via a contact hole 28, the capacitance-coupling effect generated between the pixel electrode 26 and the data line 22 is the same as that generated between the source electrode 20c and the data line 22. Further, the distance between the source electrode 20c and the data line 22, located at the same mask, is constant, and the edge of the pixel electrode 26 is located above the source electrode 20c and located within the range of the source electrode 20c. Despite the distance between the source electrode 20c and the data line 22 being slightly uneven during the formation of the pixel electrode 26, the capacitance-coupling effect generated between the pixel electrode 26 and the data line 22 remains the same, based on the constant distance between the source electrode 20c and the data line 22.

Fig. 3A is a plan view showing the structure of one pixel of a TFT structure according to another embodiment of the present invention.

The TFT array structure comprises a Thin-Film Transistor 20, a data line 22, a scanning line 24, a pixel electrode 26 and an auxiliary electrode 30. The data line 22 is connected to the drain 20a of the Thin-Film Transistor 20, and the scanning line 24 is connected to the gate 20b of the Thin-Film Transistor 20. The scanning line

ANNEX B

1. (Once amended)
A Thin-Film Transistor array structure, comprising:
a Thin-Film Transistor;
a data line coupled to a drain electrode of the Thin-Film Transistor;
a scanning line coupled to a gate electrode of the Thin-Film Transistor and crossed to the data line to form a plurality of rectangular pixels in matrix;
a pixel electrode formed at each of the pixels and coupled to a source electrode of the Thin-Film Transistor , the pixel electrode having an edge; and
an [sustaining] auxiliary electrode coupled to the pixel electrode. [disposed on the pixel electrode] and next to the data line [and coplanar with the source electrode] , wherein the edge of the pixel electrode is disposed on the auxiliary electrode.

2. (Once amended)
The Thin-Film Transistor array structure as claimed in Claim 1, wherein a pattern constructed by the [sustaining] auxiliary electrode, the source electrode and the data line is designed as a mask.

3. (Once amended)
The Thin-Film Transistor array structure as claimed in Claim 1, wherein the [sustaining] auxiliary electrode is formed in an H-shaped pattern.

4. (Once amended)
The Thin-Film Transistor array structure as claimed in Claim 1, wherein the pixel electrode is coupled to the [pixel] source electrode via a contact hole.

5. (Once amended)
The Thin-Film Transistor array structure as claimed in Claim 1, wherein the [sustaining] auxiliary electrode is coupled to the pixel electrode via a contact hole.

6. (Once amended)
A Thin-Film Transistor array structure, comprising:
a Thin-Film Transistor;
a data line coupled to a drain electrode of the Thin-Film Transistor;
a scanning line coupled to a gate electrode of the Thin-Film Transistor and crossed to the data line to form a plurality of rectangular pixels in matrix; and
a pixel electrode formed at each of the pixels and coupled to a source electrode of the Thin-Film Transistor via a contact hole, wherein the edge of the pixel electrode is disposed on the source electrode which is extended to the region where the pixel electrode is next to the data line.